LM TECHNOLOGIES®

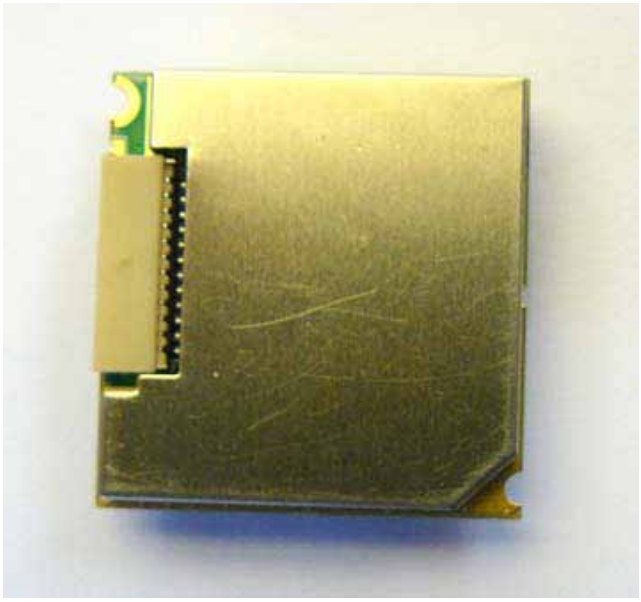
INNOVATIVE TECHNOLOGY PRODUCTS

LM477

Based on the high performance features of the SiRF StarIII low power single chipset
Cold/Warm/Hot start time: 42/38/1 sec. at open sky and stationary environments
Very high sensitivity (tracking sensitivity: -159 dBm)
RF Metal Shield for best performance in noisy environments
TTL level serial port for GPS communications interface
Protocol: NMEA-0183/SiRF Binary (default NMEA)
Baud Rate: 4800, 9600, 19200, 38400 or 57600 bps (default 9600)
Secure SMD PCB mounting method

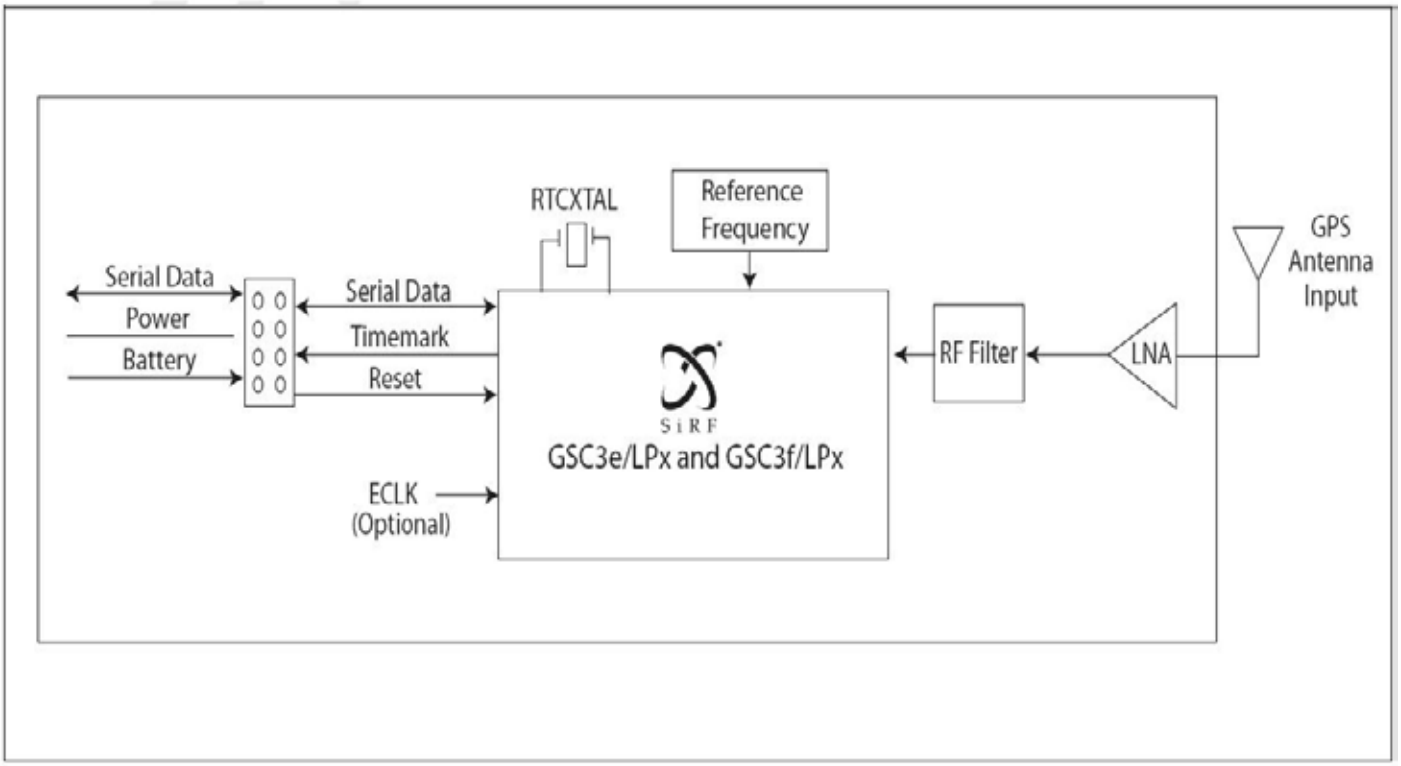
Features

- SiRF Star III chipset
- Low Power: Under 60mW at full power / 46mW tracking power
- 3.0V to 3.6V operation
- High sensitivity for indoor fixes
- Support 20-channel GPS
- Real-time navigation for location-based services
- Multi-standard support: 3G PP,3GPP2,PDC,iDEN and TIA-916
- Multi-mode: Mobile centric to network cenPtric
- Interface: 2 UARTs& 1 GPIO
- RoHS Compliant
- On Board Capacitor (0.08F) for RT C, Over 30 minutes back-up power
- Mini outline: 29 X 26 X 8.4 mm (With Patch Antenna)



0207 428 2647 | www.lm-technologies.com | business@lm-technologies.com

Block Diagram



Operating conditions

Power supply			
Parameter	**Min.**	**Max.**	**Unit**
VRTC	3.3	4.2	DCV
VIN	2.85	3.6	DCV
BOOTSEL	2.7	3.6	DCV
Temperature			
operating	-10°C ~ 60°C (14°F ~ 140°F)		
storage	-20°C ~ 70°C (-4°F ~ 158°F)		
humidity	Operational up to 95% non-condensing		

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GPS Specification

Electrical Characteristics	
GPS Chipset	SiRF Star Ⅲ
Frequency	L1, 1575.42 MHz
C/A Code	1.023 MHz chip rate
Channels	20 channel all-in-view tracking
Accuracy	
Position Horizontal	10 meters, 2D RMS 1-5 meters 2D RMS, WAAS corrected
Velocity	0.1m/sec
Time	1 micro-second synchronized to GPS time
Datum	
Datum	Default: WGS-84
Acquisition Rate	
Hot start	1 sec., average
Warm start	38 sec., average
Cold start	42 sec., average
Reacquisition	0.1 sec. average
Protocol	
GPS Protocol	Default: NMEA 0183 (Secondary: SiRF binary)
GPS Output format	GGA(1sec), GSA(1sec), GSV(5sec), RMC(1sec), GLL, VTG is optional
Dynamic Condition	
Altitude Limit	18,000 meters (60,000 feet) max.
Velocity Limit	515 meters/sec. (1,000 knots) max.
Jerk Limit	20 m/sec**3
Acceleration Limit	Less than 4g

Operating Modes

Normal Power	**Entire chip enable (normal operation)**
Clock only	**The RF section PLL and receiver chain are disabled. All other circuits are powered. This mode is used during low power operations such as TricklePower or Advanced Power Management. It allows the GSC3e(f)/LPx to save power by shutting down portions of the RF section while it is idle and the SiRFstarIII core and ARM are still performing.**
Stand-by	**The RF section is disabled. The digital section clocks are idle. The RTC and battery back up sections are powered. This mode allows the GSC3e(f)/LPx to minimize power consumption while the chip is in an idle period such as during a power management cycle.**
Hibernate	**All circuits except the RTC and battery back-up RAM are disabled. Can wake-up at a preset time or by external interrupt Vin On-Off. This is additional function to battery back up mode.**

GPM-210 Pin Function

No.	Pin Name	Pin Type	Pin description
1	BOOTSEL	Input	Module boot mode select (leave it open normally)
2	GPIO1	Output	LED Indicator (Acquisition :one flash per second / Tracking: Always ON)
3	TX0	Output	Serial message output port for channel 0
4	RX0	Input	Serial receive port for channel 0
5	TX1	Output	Serial message output port for channel 1 (leave it open normally)
6	RX1	Input	Serial receive port for channel 1 (leave it open normally)
7	RESET	Input	Reset input (leave it open normally)
8	WAKE UP	Input	Reserved
9	TIME MARK	Output	Reserved
10	VRTC	Power	RTC power intput
11	VIN	Power	VDD power input
12	GND	GND	Common ground

GPM-210 Dimension